# Lab 3.1 Report

1. Problem analysis

In lab 3.1 we are implementing the simulator of RISCV-LC, especially the finite state machine for stage update. Different from previous code, this time we are separating each instruction into many different stages, and for each stage the 33 control signal bits will be different, and we have to implement how are the 128 states interconnected (which is the finite state machine) and in each state, what are each signals.

1. My understandings of the RISCV-LC simulator structure
2. My understanding of the instruction execution process:

The program starts with the main function. In the main function, the program first get the binary file from the console and opens it, then it starts to initialize like allocating space for memory, loading the control state into the code etc.

Then it goes into a while loop in which the get\_command function is executed and will get command from the user interface. It can show the values in specific memories or registers, and it can also execute instructions.

The execution process is handled by the run functions. It runs a specific numbers of instructions by calling the cycle() function a specific amount of times, where each time the cycle() function executes exactly one instruction.

In the cycle instruction, the core steps of the simulator are executed. The core steps are separated into 5 parts: eval\_micro\_sequencer, cycle\_memory, eval\_bus\_drivers, drive\_bus,\_datapath\_values. Which are basically to update each parts including PC, memory, BUS and so on in the microarchitecture for each instruction. These steps are determined by the control signals in the file uop.

1. My understanding of the finite state machine

There are 22 states in the finite state machine in total, but these ID (state number) are from 0 to 127, this is first good for future extensions, and also it is because the IR[6:0] and J6~J0 are 7 bits and is easy to map to 0 to 127. In the finite state machine graph there are 21 states, and the HALT state(127) is ignored. From the graph we can know that for each state, what processes are done and what are the next state for each state, so we can implement the uop file.

1. My understanding of the uop file

uop file is the file where we store the exact numbers of each state. It has 128 rows in total, which corresponds to the 128 states with state numbers 0 to 127. For each row, there are 33 columns, which correspond to 33 specific control signals for each states. Control signals include:

1. IRD: it determines if the state number of next state is from the instruction bits [6:0] (when IRD is 1) or from J6~J0 (together with B, READY, etc.) in ROM (when IRD is 0).
2. J6~J0: when IRD is 0, they partly determine the state transition
3. LD: they basically enable whether each structures (PC, MAR, etc.) read and update their values in the current stage or not.
4. Gate: gate are enable signals for bus tristate driver. If they are enabled (1), it means that on the bus we can read its value, otherwise we disable it (0).
5. MUX: just the selection value of each multiplexer.
6. En: the enable value of output or input for register file and memory
7. RESET: a special signal to indicate whether to reset the whole RISCV-LC.
8. My understanding of some key implementations in the code
9. Some commonly used functions and macros
10. handle\_get\_element\_of\_error(x, id):

By masking and shifting, we can get specific digits of the input, so we can use MACROS to easily get the IRD, J, B etc. values.

1. MUX function:

MUX functions are the simulator of real multiplexers. For example, int blockBMUX(int, int, int): represent the B mux: return B or 0 according to LD.BEN.

1. Some key variables
2. struct\_system\_latches:

The latch is kind of the set that stores all the values for state, including PC, registers, MAR, IR, B, READY, MICROINDTRUCTION, and STATE\_NUMBER. We have 2 struct\_system\_latches which are CURRENT\_LATCHES and NEXT\_LATCHES that stores the value of the current and next stage.

1. Handle hard-wired 0

In the code, we need to handle the hard-wired 0: which means that no matter what operation is done to REG[0], in the next stage, the REG[0] is still zero. This can be done by setting NEXT\_LATCHES.REGS[0] to 0 at the eval\_micro\_sequencer() function:

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Description automatically generated

1. Handle the uop file
2. Preprocessing of the uop file

The uop matrix is really hard to read, so I decide to convert it to an excel file so that I can quickly locate specific rows and columns. So I wrote the to\_csv.c file to convert it to csv file by adding comma in-between:

A screenshot of a computer program

Description automatically generated

And after converting, we can open it in Excel with clearer layout (with other labels in yellow and undetermined values in green):

A white sheet with black dots and yellow lines

Description automatically generated

Then, we can modify each undetermined value.

1. State 1:

A diagram of a memory

Description automatically generated

In state 1, the next state depends on the value of READY, if READY is 0, then next state is 1 (0000001if READY is 1, the next state is 5 (0000101).

A diagram of a control signal

Description automatically generated

Looking at the control part we can see, if we set J0 to 1, and all others to 0, we can achieve this purpose since if J2 is 0, it is actually READY that determines bit2.

In this stage we update MDR to the value of memory at the address of MAR.

Therefore, no PC is updated, so LD.PC is 0;

No MAR is updated, so LD.MAR is 0;

MDR is updated, so LD.MDR is 1;

In this stage, we don’t need to read the values from register file, so RS1EN and RS2EN should both be disabled, set to 0. The RS2MUX should be set to 0 to choose the output of rs2 because in this stage, we don’t want to calculate with ALU and the 2 inputs of the ALU should be disabled. But there is no control for disabling the I immediate generator, so we can only let the RS2MUX choose the disabled RS2 to make the input disabled.

Since we want to read the data from memory to MDR, we should make the memory IO enabled, by setting MIO\_EN to 1.

1. State 2

A diagram of a memory

Description automatically generated

State 2 is almost the same with state 1, the only difference is that if READY is 0, then next state is 2 (0000010if READY is 1, the next state is 6 (0000110).

Looking at the control part we can see, if we set J1 to 1, and all others to 0, we can achieve this purpose since if J2 is 0, it is actually READY that determines bit2.

1. State 32

A diagram of a computer code

Description automatically generated with medium confidence

The next state is 33 (0b 0100001) so J0 and J5 should be set to 1, others 0.

This state, we load the value of rs2 into MDR, therefore,

No PC is updated, so LD.PC is 0;

No MAR is updated, so LD.MAR is 0;

MDR is updated, so LD.MDR is 1;

No instruction is updated, so LD.IR is 0;

No register is updated, so LD.REG is 0.

Since the next state number doesn’t depend on the value of B, so in the multiplexer we set LD.BEN to 0 meaning that we won’t choose the B value to determine the control signal.

For the tristate driver gates, since in this stage the value on the bus is the value of rs2, so only the gate that controls RS2 value should be enabled and all other values are disabled. Meaning that GatePC, GateMAR, GateMDR, GateALUSHF are set to 0, and GateRS2 is set to 1.

Since PC is not updated at this stage, so in theory we don’t need to determine the values of PCMUX, ADDR1MUX, ADDR2MUX because the LD.PC is disabled and these values are not used. But in practice, we set them to the default value, which is 0, meaning that PCMUX=0, ADDR1MUX, ADDR2MUX = 00.

Since the GateMAR is disabled, actually the value of MARMUX is unused and in theory we don’t need to use the value determined by MARMUX, but in practice, we set it to the default value, which is 0, meaning that MARMUX=0.

Since the value of MDR comes from the value of rs2 in the BUS, so that the input of MDR should be from the bus, so that MDRMUX should be 1 to choose from the BUS.

In this stage, we don’t need the value of Selection Logic part, so in theory the input of the ALU determined by RS2MUX doesn’t have to be determined, but in practice, we set it to default 0.

1. State 33

A diagram of a number

Description automatically generated

In state 33, the next stage determination is almost the same with state 1, the only difference is that if READY is 0, then next state is 33 (0100001) if READY is 1, the next state is 37 (0100101).

Looking at the control part we can see, if we set J1 and J5 to 1, and all others to 0, we can achieve this purpose since if J2 is 0, it is actually READY that determines bit2.

In this state, we load the value of MDR to the memory at the address MAR, therefore, no register is updated, so LD.REG is 0;

Since the next state number doesn’t depend on the value of B, so in the multiplexer we set LD.BEN to 0 meaning that we won’t choose the B value to determine the control signal.

For the tristate driver gates, since in this stage no value on the bus is needed to be transfered, so all gates should be disabled. Meaning that GatePC, GateMAR, GateMDR, GateALUSHF and GateRS2 are set to 0.

Since PC is not updated at this stage, so in theory we don’t need to determine the values of PCMUX, ADDR1MUX, ADDR2MUX because the LD.PC is disabled and these values are not used. But in practice, we set them to the default value, which is 0, meaning that PCMUX=0, ADDR1MUX, ADDR2MUX = 00.

Since the GateMAR is disabled, actually the value of MARMUX is unused and in theory we don’t need to use the value determined by MARMUX, but in practice, we set it to the default value, which is 0, meaning that MARMUX=0.

Since we don’t need to load anything to the MDR, so in theory we don’t need to determine MDRMUX, but in practice, we set it to the default value, which is 0, meaning that MDRMUX=0.

Since we don’t need to output anything from the register file, so we disable the output of rs1 and rs2, meaning that RS2EN and RS1EN are set to 0.

The RS2MUX should be set to 0 to choose the output of rs2 because in this stage, we don’t want to calculate with ALU and the 2 inputs of the ALU should be disabled. But there is no control for disabling the I immediate generator, so we can only let the RS2MUX choose the disabled RS2 to make the input disabled.

Since we need to modify the memory, so that MIO is enabled, meaning that MIO\_EN is set to 1, and since we need to write to memory, WE is enabled, set to 1.

Since the bit width should be selected by the control signal, the DATASIZE multiplexer should be set to 1.

1. State 51

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Description automatically generated

Since the next state of this state does not depend on the instruction, we don’t need to read from the IR[6:0] and the IRD is set to 0.

Since the next state number is 0, then we should set all J6~J0 to 0 to represent 0.

In this state, we update the rd to be the value calculated by the operation on rs1 and rs2, therefore,

No PC is updated, so LD.PC is 0;

No MAR is updated, so LD.MAR is 0;

No MDR is updated, so LD.MDR is 0;

No instruction is updated, so LD.IR is 0;

Register file is updated, so LD.REG is 1.

Since the next state number doesn’t depend on the value of B, so in the multiplexer we set LD.BEN to 0 meaning that we won’t choose the B value to determine the control signal.

For the tristate driver gates, since in this stage the value on the bus is the value of the ALU, so only the gate that controls Selection logic value should be enabled and all other values are disabled. Meaning that GatePC, GateMAR, GateMDR, GateRS2 are set to 0, and GateALUSHF is set to 1.

Since PC is not updated at this stage, so in theory we don’t need to determine the values of PCMUX, ADDR1MUX because the LD.PC is disabled and these values are not used. But in practice, we set them to the default value, which is 0, meaning that PCMUX=0, ADDR1MUX=00.

Since in this stage we need to calculate the values by ALU based on the output of rs1 and rs2, so we should enable RS2EN and RS1EN, setting them to 1.

Since the input value of ALU is rs1 and rs2, so in the RS2MUX we should choose the value from RS2, setting the value of RS2MUX to 0.

Since in this stage, no memory operation is needed, so we should set MIO\_E and WE to 0. Since we don’t select the bitwidth because no memory operation is performed, we set it to 0 by making the multiplexer choose 0 (setting the DATASIZE to 0)

Since in this state we don’t reset the RISCV-LC, we do not enable reset, setting RESET to 0.

1. State 102

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Description automatically generated

Since the next state of this state does not depend on the instruction, we don’t need to read from the IR[6:0] and the IRD is set to 0.

Since the next state number is 0, then we should set all J6~J0 to 0 to represent 0.

In this state, we update the value of PC to the value of the sum of rs1 + imm12, therefore,

PC is updated, so LD.PC is 1;

No MAR is updated, so LD.MAR is 0;

No MDR is updated, so LD.MDR is 0;

No instruction is updated, so LD.IR is 0;

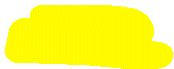
No Register file is updated, so LD.REG is 0.

Since the next state number doesn’t depend on the value of B, so in the multiplexer we set LD.BEN to 0 meaning that we won’t choose the B value to determine the control signal.

For the tristate driver gates, since in this stage the PC value are calculated by the ALU with input immediate generator and rs1, so it should be the ALU below (highlighted in yellow):

A diagram of a flowchart

Description automatically generated



Since the output of this ALU should be transferred to the BUS by GateMAR then to the PC, so only the gate that controls GateMAR value should be enabled and all other values are disabled. Meaning that GatePC, GateALUSHF, GateMDR, GateRS2 are set to 0, and GateMAR is set to 1.

Since the PC is receiving the value from the addition result of imm and rs1 instead of from PC+4, so the PCMUX should be set to 1.

Since the immediate value is the 12 bits immediate from I instruction (for example, jalr), the immediate value should be generated from I Imm Gen, so the ADDR2MUX should select the value of 1, or 01. Since the other value fed into the ALU is rs1, so that the ADDR1MUX should choose the value of 2, or 10.

Since the calculation result is from the ALU highlighted in yellow, the MARMUX should be set to 0.

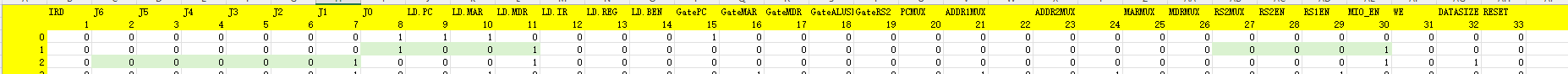
Since we don’t need to load anything to the MDR, so in theory we don’t need to determine MDRMUX, but in practice, we set it to the default value, which is 0, meaning that MDRMUX=0.

Since we only need the output of rs1 and don’t need the output of rs2, we only need to set RS1EN to 1 and set RS2EN to 0.

Since in this stage, no memory operation is needed, so we should set MIO\_E and WE to 0.

1. Final result of uop:

State 1 and 2



State 32 and 33



State 51



State 102



The final uop file:

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A screenshot of a computer

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A screenshot of a computer

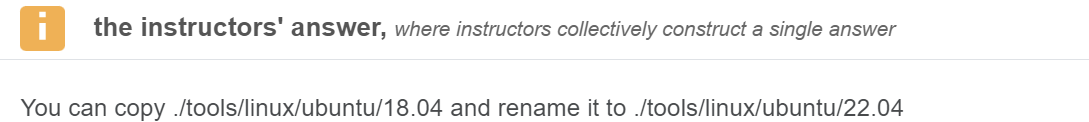
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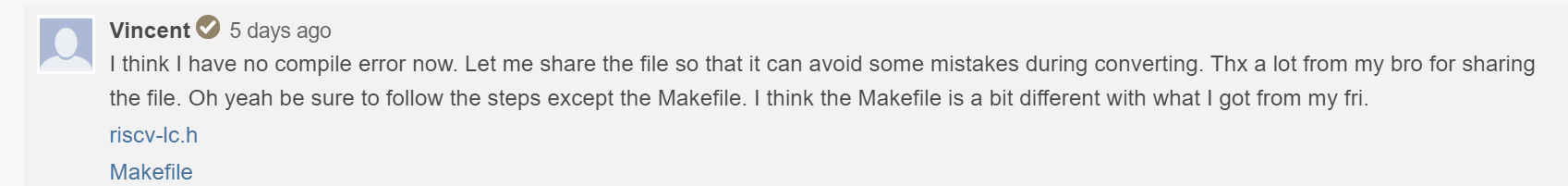
1. My mistakes and understandings

When compiling, I got this mistake:



I checked on the piazza, and I found that it is the problem that the version of my ubuntu isn’t correct. So I followed this instruction and modified my path and Makefile, and the problem is solved.





1. Console results
2. Make:

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There are some warnings but it turns out to be some version issues and is about the unsafe use of some string manipulation functions, so we can ignore it in this assignment.

1. Isa.bin

Running:

A screen shot of a computer

Description automatically generated

A screen shot of a computer

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A screenshot of a computer program

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Result:

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A screenshot of a computer

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1. Count10

Running

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A screen shot of a computer

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Description automatically generated

A black screen with white text

Description automatically generated

A black and white screen

Description automatically generated

A black screen with white text

Description automatically generated

Result

A screenshot of a computer

Description automatically generated

1. Swap

Before

A screen shot of a computer

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Running

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Description automatically generated

A black screen with white dots

Description automatically generated

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Description automatically generated

Result:

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Description automatically generated

1. Add4

Before:

A screenshot of a computer

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Running:

A black and white screen

Description automatically generated

A black screen with white text

Description automatically generated

A black screen with white text

Description automatically generated

A screen shot of a computer

Description automatically generated

A screen shot of a computer

Description automatically generated

Result:

A black screen with white text

Description automatically generated

# Reference:

TextBook -Computer Organization and Design\_ The Hardware Software Interface [RISC-V Edition]

opcodes-rv32i reference document

risc-v-asm-manual.pdf

riscv-spec-20191213.pdf

fsm.pdf

riscv-lc.pdf